Part II

Devices – Diode, BJT, MOSFETs

4

Semiconductor

- Semiconductor
  - The number of charge carriers available to conduct current[1] is between that of conductors and that of insulators.
  - Semiconductor is basically a *pn* junction where the *p*-type silicon contacts with the *n*-type silicon.
    - Different types of silicon are created by implanting different dopings.

4.1 Intrinsic Silicon

- Figure 4.1 shows the 2-D structure of the intrinsic silicon.
  - Each atom shares each of its 4 valence electrons with a neighboring atom.
  - Atoms are held in their positions by covalent bounds.
    - Covalent bounds are intact at sufficient low temperature.
      - No free electrons are available to conduct current.
    - Covalent bounds may be broken by thermal ionization.
- Thermal ionization at room temperature (Figure 4.2)
  - An electron leaves its parent atom; thus, a positive charge is left with the atom.
    - The ionization results in free electrons and holes in equal numbers.
    - At room temperature, the silicon has 1.5×10^{10} carries/cm^3 and about 5×10^{22} atoms/cm^3.
      - The concentration of free electrons n is equal to the concentration of free holes p.

$$n = p = n_i \tag{4.1}$$

      - n_i is the number of free electrons (or holes) per cm^3 in intrinsic silicon at a given temperature.

$$n_i^2 = BT^3 e^{-E_G/kT} \tag{4.2}$$

[1] The current of 1 ampere is defined as 1 coulomb of electric charge (which consists of about 6.242×10^{18} electrons) drifts every second at the same velocity through the imaginary plane through which the conductor passes.

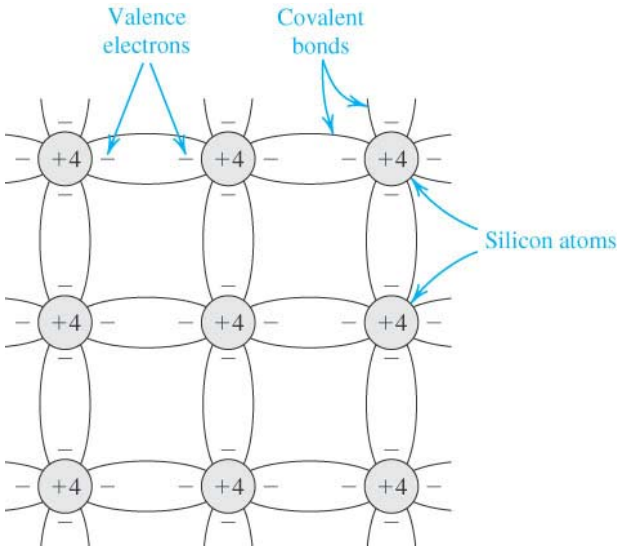


Figure 4.1: Two-dimensional representation of the silicon crystal.

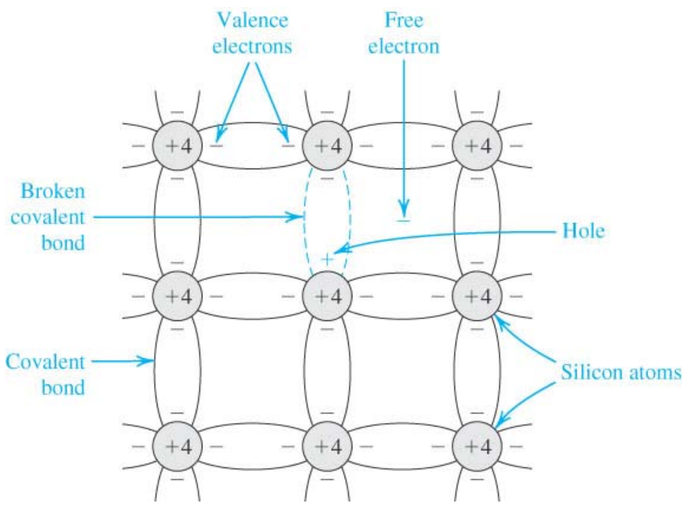


Figure 4.2: Electrons and holes generated by thermal ionization.

- B is a material dependent parameter= 5.4×10^{31} for silicon.
- E_G is the bandgap energy=1.12 electron volts (eV), representing the minimum energy required to break a covalent bound and generate an electron-hole pair.
- k is Boltzmann's constant $= 1.38 \times 10^{-23}$ joules/kelvin.
- T is absolute temperature in Kelvins $= 273 +$ temperature in °C.

– An electron from a neighboring atom may be attracted and create a new hole.
  * Ionization rate is equal to recombination rate in thermal equilibrium.

– The process repeats with a hole moves through the silicon and conducts current.

* Holes and electrons move through silicon by diffusion and drift mechanisms.

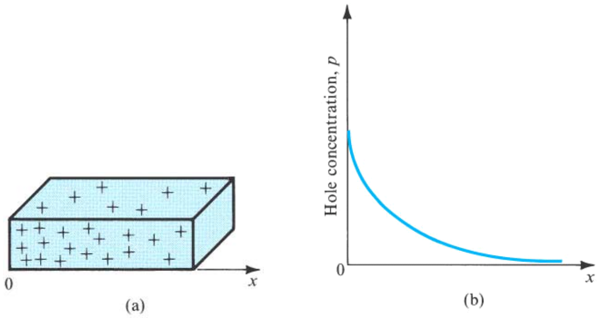


Figure 4.3: Illustration of diffusion mechanism: (a) a bar of intrinsic silicon, and (b) the hole concentration profile.

- Diffusion mechanism
  - Random motion due to thermal agitation.
  - Non-uniform concentrations of free electrons and holes cause a net flow of charge (or diffusion current).
  - The current density of the hole diffusion current at any point.

$$J_p = -qD_p \frac{dp}{dx} \tag{4.3}$$

    * J_p in A/cm^2 is the current density, i.e., the current per unit area of the plane perpendicular to the x-axis.[2]
    * p is the concentration of free holes.
    * q is the magnitude of electron charge= $1.6 \times 10^{-19}C$.
    * D_p is the diffusion constant of holes=$12 cm^2/s$.
    * A negative (dp/dx) results in a positive current in the x direction.
  - The magnitude of the electron diffusion current at any point.[3]

$$J_n = qD_n \frac{dn}{dx} \tag{4.4}$$

    * J_n in A/cm^2 is the current density, i.e., the current per unit area of the plane perpendicular to the x-axis.
    * n is the concentration of free electrons.
    * q is the magnitude of electron charge= $1.6 \times 10^{-19}C$.
    * D_n is the diffusion constant of electrons=$34 cm^2/s$.

[2] The unit of J_p can be derived from the formulation $J_p = -q(\text{charge})D_p(\text{cm}^2/\text{s})dp(\text{difference of the number of the holes/cm}^3)/dx(\text{cm}) = (\text{charges/s})/\text{cm}^2 = \text{A/cm}^2$.

[3] To double check.

        * A negative (dn/dx) results in a negative current in the x direction.
- Drift mechanism
    - Carrier drift occurs when an electric field is applied across a piece of silicon.
    - Free electrons and holes are accelerated by electric field and acquire a drift velocity (superimposed on the velocity of thermal motion).

$$v_{drift} = u_p E \tag{4.5}$$

        * u_p is the mobility of holes in cm^2/V·s = 480.
        * E is the strength of electric field in V/cm.
    - The current density of holes in A/cm^2.

$$J_{p-drift} = qpu_p E \tag{4.6}$$

    - The current density of electrons in A/cm^2.

$$J_{n-drift} = qnu_n E \tag{4.7}$$

        * u_n is the mobility of electrons in cm^2/V·s = 1350.
    - The total drift current density in A/cm^2.

$$J_{drift=}q(pu_p + nu_n)E \tag{4.8}$$

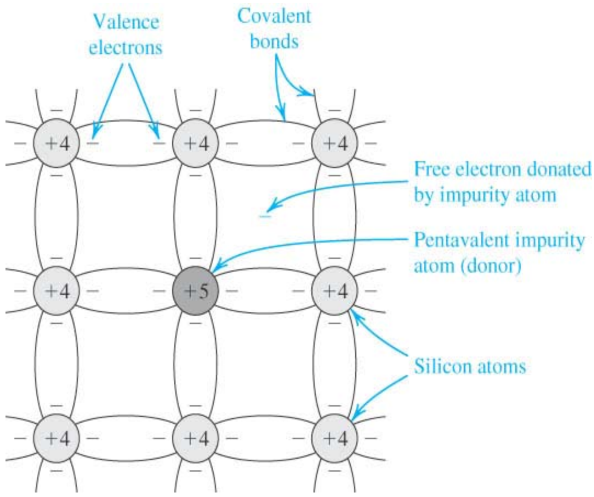
        * A form of Ohm's law with the resistivity $\rho = 1/q(pu_p + nu_n)$ in $\Omega \cdot cm$.
- Einstein relationship

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = V_T \tag{4.9}$$

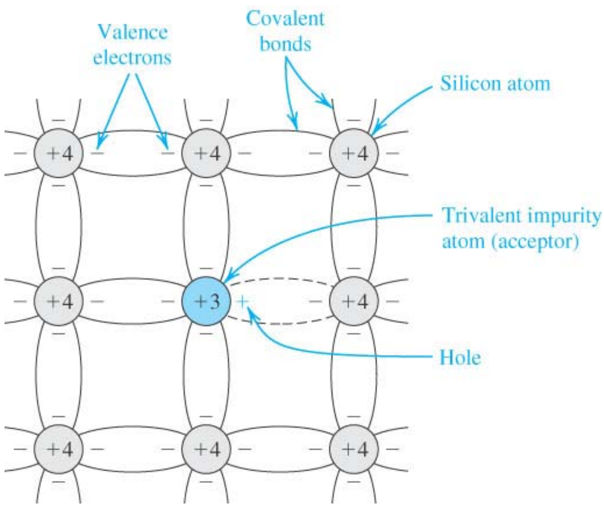
4.2 Doped Silicon

- Doped silicon
    - Achieved by introducing a small number of impurity atoms.
- In n-type silicon, the majority of carriers are the negatively charged electrons.
    - Achieved by implanting pentavalent impurity (also known as donor).
    - In thermal equilibrium
        * The concentration of free electrons $n_{n0} \simeq N_D$.
        * The product of electron and hole concentrations remains constant.
            · p_{n0} is a function of temperature.

$$n_{n0} p_{n0} = n_i^2 \tag{4.10}$$



(a) n-type



(b) p-type

Figure 4.4: Doped n-type and p-type semiconductor.

- In p-type silicon, the majority of carriers are the positively charged holes.
  - Achieved by implanting trivalent impurity (also known as acceptor).
  - In thermal equilibrium
    - The concentration of free holes $p_{p0} \simeq N_A$.
    - The product of electron and hole concentrations remains constant.
      - n_{p0} is a function of temperature.

$$n_{p0}p_{p0} = n_i^2 \tag{4.11}$$

- A piece of p-/n-type silicon is electrically neutral.
  - The majority of free carriers are neutralized by bound charges associated with impurity atoms.

5

Diode

A two-terminal device with a nonlinear $i - v$ characteristic.

- Main applications
  - Rectifier.
  - Generation of DC voltages from AC power.
  - Generation of signals of various waveforms.
- Circuit symbol

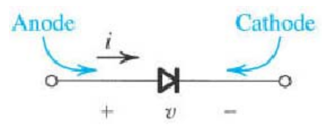


Figure 5.1: The symbol of diode.

5.1 Physical Structure

- Diode is basically a *pn* junction device.

5.1.1 The *pn* Junction Under Open Circuit

- Figure 5.2 shows the *pn* junction with open circuit.
- Diffusion current I_D.
  - Generated by the movement of majority carriers.
  - Electrons diffuse across the junction from the n side to the p side.
  - Holes diffuse across the junction from the p side to the n side.
  - The two currents add together to form a diffusion current I_D with direction from p side to n side.
- Depletion region.
  - Electrons diffuse across the junction and combine with majority holes.

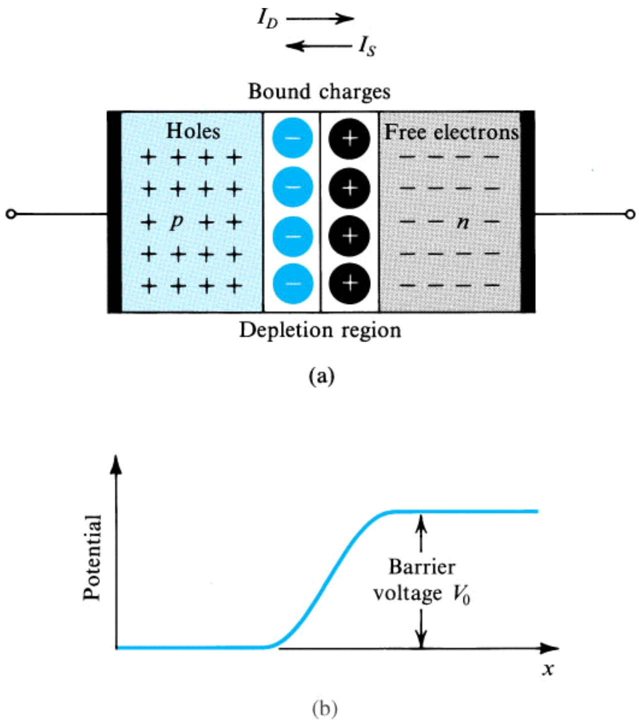


Figure 5.2: (a) The pn junction with no applied voltage (open-circuited terminals). (b) The potential distribution along an axis perpendicular to the junction.

  * In p-type silicon, there will be a region depleted of holes and containing uncovered bound negative charge.
- Holes diffuse across the junction and combine with majority electrons.
  * In n-type silicon, there will be a region depleted of electrons and containing uncovered bound positive charge.
- The bound charges on both sides of the depletion region forms a junction built-in voltage.

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{5.1}$$

  * N_A and N_D are the doping concentrations of the p side and the n side, respectively.
  * The built-in voltage V_0 for silicon at room temperature is $0.6 \sim 0.8V$.
  * The electric field acts as a barrier that must be overcome for holes and electrons to diffuse.
- Depletion regions exist in both sides with equal among of charges.
  * The depletion layer will extend deeper into the more lightly doped material.

$$\begin{aligned} q x_p A N_A &= q x_n A N_D \\ \frac{x_n}{x_p} &= \frac{N_A}{N_D} \end{aligned} \tag{5.2}$$

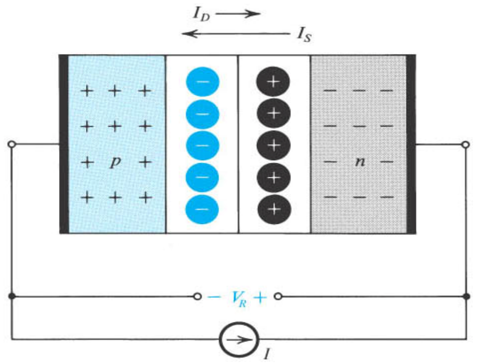


Figure 5.3: The pn junction excited by a constant-current source I in the reverse direction. To avoid breakdown, I is kept smaller than IS. Note that the depletion layer widens and the barrier voltage increases by VR volts, which appears between the terminals as a reverse voltage.

* The width of the depletion region of an open-circuit junction is typically in the range of 0.1um to 1um.

$$W_{dep} = x_n + x_p = \sqrt{\frac{2\varepsilon_s}{q}(\frac{1}{N_A} + \frac{1}{N_D})V_0} \tag{5.3}$$

- Drift current $I_{S_{drift}}$.
  - Achieved by the movement of thermally generated minority carriers.
  - Electrons in p-silicon diffuse to the depletion region and got swept to the n-silicon.
  - Holes in n-silicon diffuse to the depletion region and got swept to the p-silicon.
  - The two currents add together to form a drift current $I_{S_{drift}}$ with direction from n side to p side.
  - $I_{S_{drift}}$ depends on temperature instead of the built-in voltage V_0.
- In thermal equilibrium and under open circuit condition, $I_{S_{drift}} = I_D$.
  - If $I_D > I_{S_{drift}}$, the uncovered bound charges will increase and the voltage across the depletion region will increase. This in turn causes I_D to decrease.
  - If $I_{S_{drift}} > I_D$, the uncovered bound charges will decrease and the voltage across it will decrease. This in turn causes $I_{S_{drift}}$ to decrease.

5.1.2 The *pn* Junction Under Reverse-Bias

- Figure 5.3 depicts the pn junction with reverse bias.
- Electrons flows from the n-side to the p-side through the external circuit.
  - Electrons leaving the n-side cause an increase in the positive bound charges.
  - Holes leaving the p-side cause an increase in the negative bound charges.

- A increase in the width of, and the charges stored in, the depletion region.
  - A higher barrier voltage results in the decrease of I_D.
- In thermal equilibrium, $I_{S_{drift}} - I_D = I$.

- Depletion capacitance
  - As the voltage across the pn junction changes, the charges stored in the depletion layer changes.[1]
  - The charges q_J stored in the depletion layer.
    - A function of V_R.
    - A is the cross-sectional area of the junction.

$$
\begin{aligned}
q_J &= q_N \\
&= qN_D x_n A \\
&= q\frac{N_D N_A}{N_D + N_A} W_{dep} A \\
&= q\frac{N_D N_A}{N_D + N_A} A \sqrt{\frac{2\varepsilon_s}{q}(\frac{N_A + N_D}{N_A N_D})(V_0 + V_R)}
\end{aligned}
\tag{5.4}
$$

  - The depletion capacitance.

$$
C_j = \frac{dq_J}{dV_R} = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{V_0}}} \tag{5.5}
$$

    - The capacitance varies with the bias point.
    - C_{j0} is the value of C_j with no voltage applied.

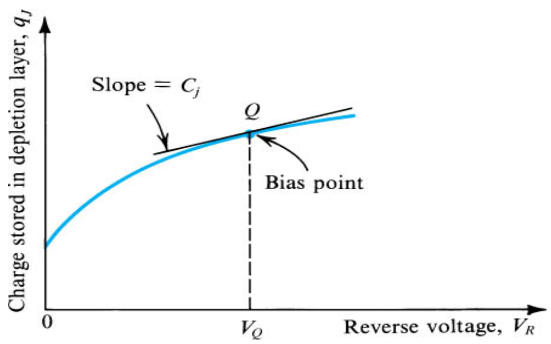


Figure 5.4: The charge stored on either side of the depletion layer as a function of the reverse voltage VR.

[1]Capacitance $C = \Delta Q/\Delta V$.

5.1.3 The *pn* Junction in the Breakdown Region

- A sufficiently high junction voltage develops and many carriers are created by zener or avalanche mechanism so as to support any value of reverse current.
  - It is not a destructive process as long as the maximum power dissipation is not exceeded.
- Zener effect
  - It occurs when the breakdown voltage $V_Z < 5V$.
  - Electric field in the depletion regions increases to a point where it can break covalent bounds and generate electron-hole pairs.
    * The holes will be swept into the n side.
    * The electrons will be swept into the p side.
    * These electrons and holes constitute a reverse current across the junction.
- Avalanche effect
  - It occurs when the breakdown voltage $V_Z < 7V$.
  - Minority carriers gain sufficient energy by the electric field to break the covalent bounds.
    * The carriers may have sufficient energy to cause other carriers to be liberated in another ionizing collision.

5.1.4 The *pn* Junction Under Forward Bias Conditions

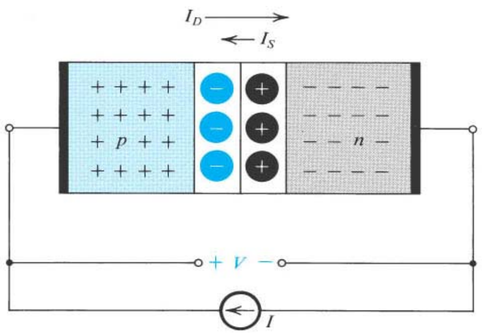


Figure 5.5: The pn junction excited by a constant-current source supplying a current I in the forward direction. The depletion layer narrows and the barrier voltage decreases by V volts, which appears as an external voltage in the forward direction.

- Figure 5.5 depicts the *pn* junction with forward bias.
- The barrier voltage is reduced since majority carriers neutralize some of the uncovered bound charge.
  - Majority carriers are supplied to both sides through the external circuit.
  - Holes are injected into the n-side and electrons are injected into the p-side.

* The concentration of minority carriers at both sides will exceed the thermal equilibrium, p_{n0} and $n_{p0.}$
* The excess concentration decreases exponentially as one moves away from the junction.
* In the steady state, the concentration profile of excess minority carriers remains constant.

– Diffusion current I_D increases until the equilibrium is achieved with $I_D - I_{S_{drift}} = I$.

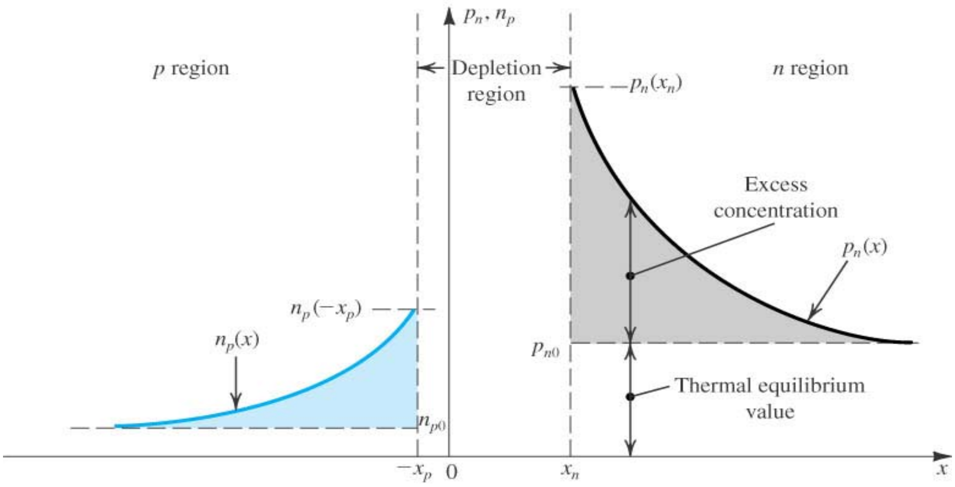


Figure 5.6: Minority-carrier distribution in a forward-biased pn junction. It is assumed that the p region is more heavily doped than the n region.

- Diffusion capacitance
  – In steady state, a certain amount of excess minority-carrier charge is stored in each of the p and n bulk region. If the terminal voltage changes, this charge will have to change before a steady state is achieved.

$$C_d = \frac{\tau_T}{V_T} I \tag{5.6}$$

* τ_T is the mean transit time of the diode, which is related to the excess minority carrier life time τ_p and τ_n.
* I is the diode current.
  · The diffusion capacitance is negligibly small when the diode is reverse bias.

- Depletion capacitance
  – As the voltage across the pn junction changes, the chargee stored in the depletion layer changes.

$$C_j = 2C_{j0} \tag{5.7}$$

5.2 Characteristics

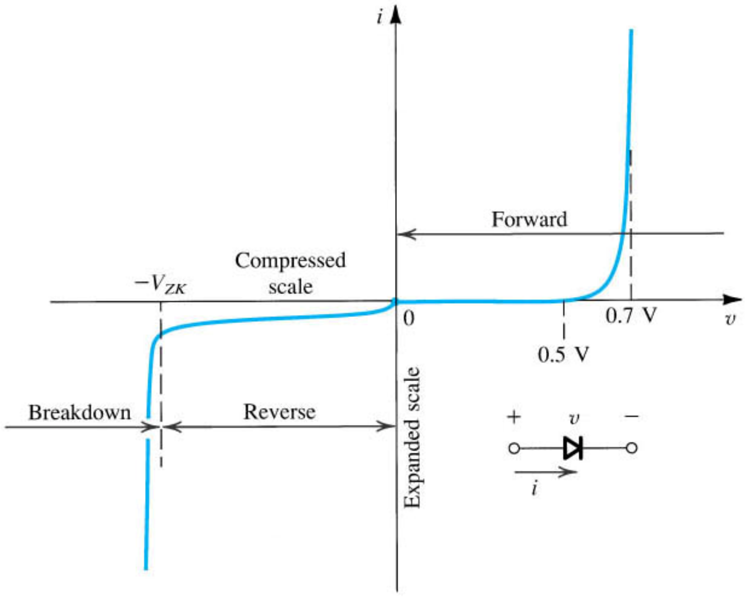


Figure 5.7: The diode $i - v$ relationship with some scales expanded and others compressed.

5.2.1 Forward Bias

- Forward region of operation is entered when the terminal voltage v is positive.
- The $i - v$ curve in forward region is closely approximated by

$$i = I_S(e^{v/nV_T} - 1) \tag{5.8}$$

  – I_S is called saturation current (or scale current).

$$I_S = Aqn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) \tag{5.9}$$

    * A function of temperature.
      · n_i is the concentration of electrons in intrinsic silicon, which depends on the temperature as suggested by Eq. (4.2).
      · Generally, I_S doubles in value for every 5 °C rise in temperature.
    * A factor proportional to the cross-sectional area of the diode.
      · A is the cross-sectional area of the pn junction.

- V_T is called thermal voltage, which is $\backsimeq$ 25mV in room temperature (20 °C).

$$V_T = \frac{kT}{q} \tag{5.10}$$

  - k = Boltzmann's constant = 1.38×10^{-23} joules/kelvin.
  - T = Absolute temperature in Kelvins = 273 + temperature in °C.
  - q = Magnitude of electronic charge = 1.60×10^{-19} in coulomb.
- n is a value between 1 and 2
  - A value depends on the material and physical structure of the diode.
  - By default, $n = 1$ unless otherwise specified.

- If $i \gg I_S$, the $i - v$ curve in forward regions can be further approximated by the exponential relationship.

$$i \simeq I_S e^{v/nV_T} \tag{5.11}$$

  - The logarithmic form of $i - v$ characteristic.
    - The $v - i$ curve is a straight line on semilog paper[2] with a slope of $2.3nV_T$.

$$v \simeq nV_T \ln(\frac{i}{I_S}) = 2.3nV_T \log_{10}(\frac{i}{I_S}) \tag{5.12}$$

  - A factor of 10 increases in current leads to the increase of voltage drop by a factor of $2.3nV_T$, which is $\simeq$60mV in room temperature and with $n = 1$.

$$\begin{aligned} V_2 - V_1 &\simeq nV_T \ln(\frac{I_2}{I_1}) \\ \frac{I_2}{I_1} &\simeq e^{(V_2 - V_1)/nV_T} \end{aligned} \tag{5.13}$$

- Cut-in Voltage
  - A consequence of the exponential $i - v$ relationship.
    - When $v \ll nV_T$, the current i is negligible.
    - When $v \gg nV_T$, the current i grows exponentially. (Fully Conducting)
    - Example: Cut-in voltage V_{cut_in} in Figure 5.7 is $0.5V$.
  - Cut-in voltage varies with temperature for a given diode.
- Fully Conducting
  - The voltage v is greater than V_{cut_in} and the current i grows exponentially.
  - Voltage drop varies with temperature for a given diode.

5.2.2 Reverse Bias

- Reverse-bias is entered when the terminal voltage v is made negative.

[2]The vertical axis is a linear axis for v and the horizontal axis is a log axis for i.

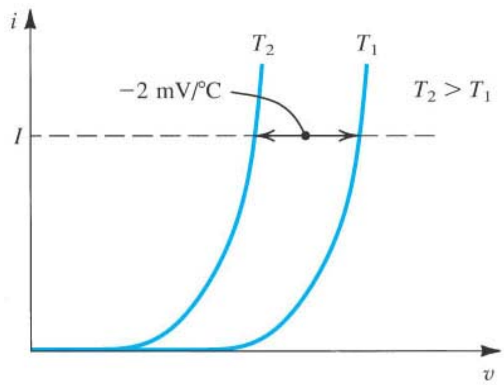


Figure 5.8: The temperature dependency of the diode forward characteristic.

- The reverse current i approximates $-I_s$.
  - The term e^{v/nV_T} in Eq. (5.8) becomes negligible as $v \longrightarrow -\infty$.
  - A function of temperature.
    - The reverse current doubles in value for every 10 °C rise in temperature.
  - A large part of reverse current is due to leakage effects.
    - Leakage currents are proportional to the junction area.
    - Real diodes exhibit reverse currents that are much larger than I_s.

5.2.3 Breakdown Region

- Breakdown region is entered when the reverse voltage exceeds breakdown voltage V_{ZK}.
- The reverse current i increases rapidly with very small increase in voltage drop.
  - A good property for voltage regulation.

5.3 Model

5.3.1 Large Signal Model

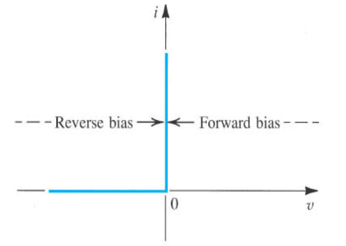
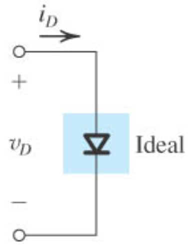
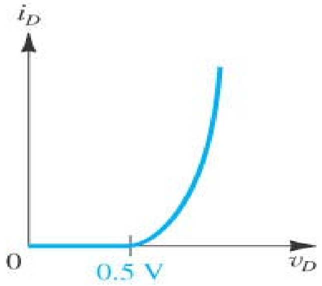
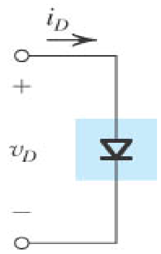
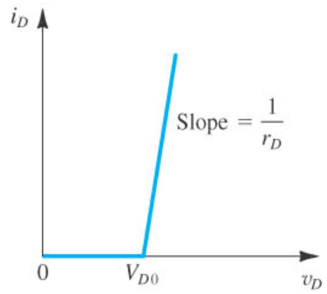
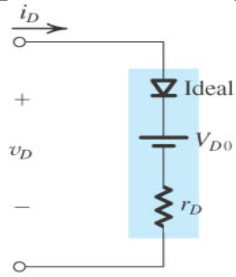
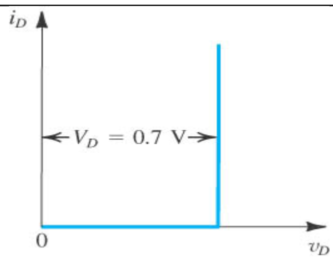
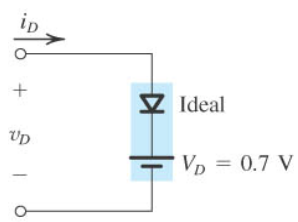
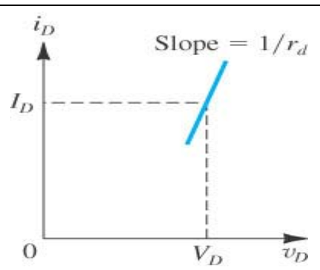
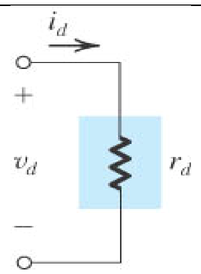
Ideal Diode

- Forward biased
  - Short circuit with zero voltage drop when $v > 0$.
- Reverse biased
  - Open circuit with zero current when $v < 0$.

Exponential Model

- The most accurate description of the diode operation in forward region.

Table 5.1: Comparison of the models in the diode forward region.

Model	$i - v$ Graph	Equivalent Circuit
Ideal		
Exponential		
Piecewise-linear	 (a)	 (b)
Constant Voltage Drop	 (a)	 (b)
Small Signal		

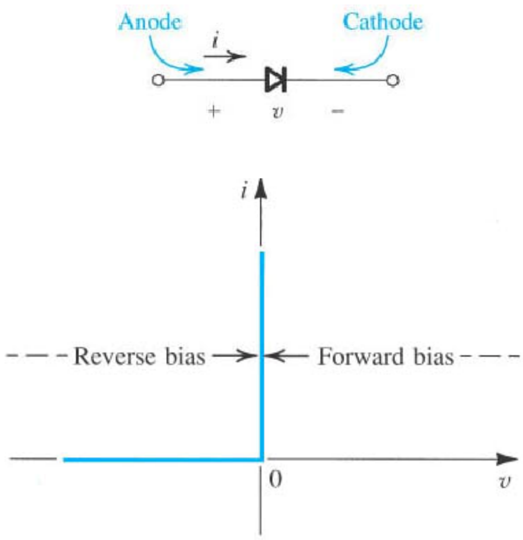
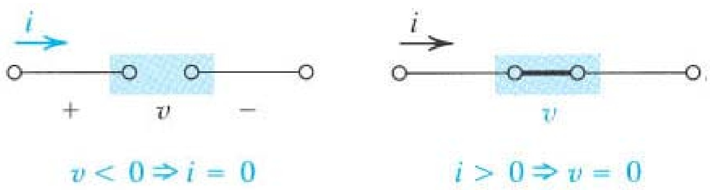


Figure 5.9: The i-v characteristic of the ideal diod.



(a) Reverse Bias (b) Forward Bias

Figure 5.10: The characteristic of the ideal diod with positive and negative voltages applied.

- The most difficult one to use due to nonlinear nature.
- Pencil-and-paper solutions: (1) graphical analysis, and (2) iterative analysis.

Example 5.1 *Given the circuit to be analyzed as in Figure 5.11, find out the I_D and V_D using graphical analysis.*

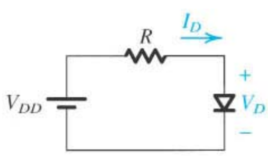


Figure 5.11: A simple circuit used to illustrate graphical analysis with exponential model.

1. Assume V_{DD} is greater than $0.5V$ so that the diode operates in forward bias region.

$$I_D = I_S e^{V_D/nV_T} \tag{5.14}$$

2. Further, writing a Kirchhoff loop equation, we can obtain the other equation that governs the circuit operation.

$$I_D = \frac{V_{DD} - V_D}{R} \tag{5.15}$$

3. Graphical analysis is performed by plotting Eq. (5.14) and Eq. (5.15) on the $i - v$ plane. The solution is the coordinate of the intersection of the two lines.
   - The line specified by Eq. (5.15) is also known as the load line.

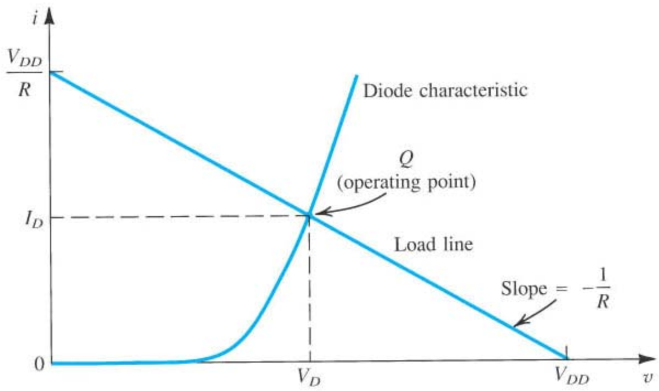


Figure 5.12: Graphical analysis for the circuit given in Figure 5.11.

Piecewise Linear Model

- A simpler model easier for analysis.

$$i_D(v_D) = \begin{cases} 0 & if \quad v_D < V_{D0} \\ (v_{D-V_{D0}})/\gamma_D & if \quad v_D \geq V_{D0} \end{cases} . \tag{5.16}$$

Constant Voltage Drop Model

- The simplest model for analysis.
  - Forward-conducting diode exhibits a voltage drop V_D of $0.7V$.
  - The model frequently employed in the initial phase of analysis and design.

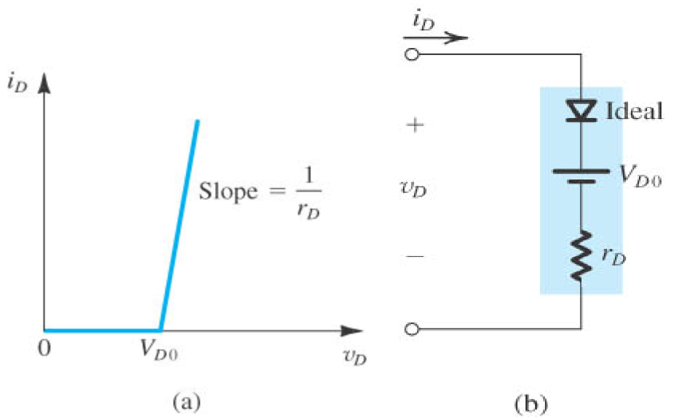


Figure 5.13: The piecewise linear model of the diod forward i-v characteristic.

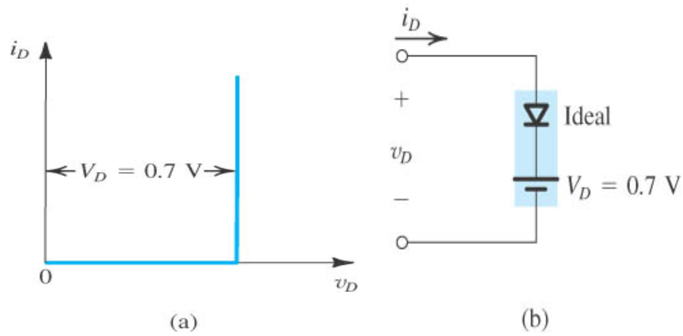


Figure 5.14: The constant voltage drop model of the diod forward i-v characteristic.

5.3.2 Small Signal Model

- Small signal model is used for the applications in which a diode is biased to operate in the forward region and a small ac signal is superimposed on the dc quantities.
- Small signal analysis
  - Determine the dc bias point (or quiescent point) using the large signal models.
    - The constant voltage drop model is commonly used.
  - Determine the small signal operation around the dc bias point by modeling the diode with a resistance.
    - The resistance is the slope of the tangent to the exponential $i - v$ curve.

Example 5.2 *Consider the circuit in Figure 5.15, where the dc voltage V_D is applied to the diode and a time varying signal $v_d(t)$ is further superimposed to the dc voltage V_D, and the corresponding graphical representation, find out the $i_D(t)$ and $v_D(t)$ of the diode.*

1. The dc operation point of the diode can be found as follows:

$$I_D = I_s e^{V_D/nV_T} \tag{5.17}$$

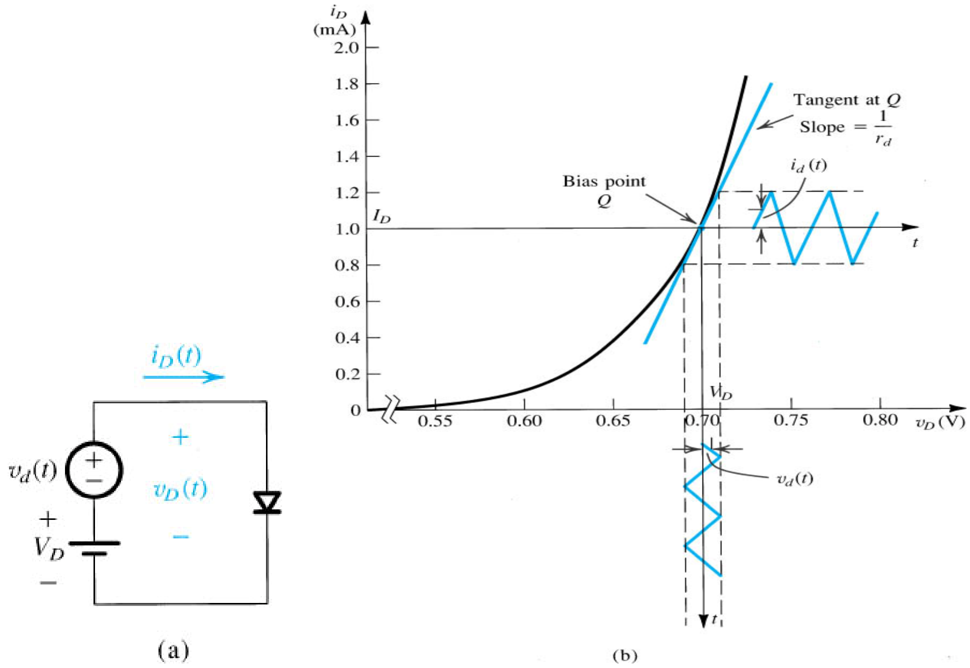


Figure 5.15: Circuit for the development of the diode small signal model and the corresponding graphical representation.

2. When the small signal $v_d(t)$ is applied, the instantaneous diode current $i_D(t)$ will be

$$\begin{aligned} i_D(t) &= I_s e^{(V_D + v_d(t))/nV_T} \\ &= I_s e^{V_D/nV_T} \times e^{v_d(t)/nV_T} \\ &= I_D \times e^{v_d(t)/nV_T} \end{aligned} \tag{5.18}$$

3. If the amplitude of the signal $v_d(t)$ is kept sufficiently small, the exponential term in Eq. (5.18) can be expanded in a series.[3] The small signal approximation is obtained by truncating the series after the first two terms.

$$i_D(t) = I_D \times e^{v_d(t)/nV_T} \simeq I_D \times \left(1 + \frac{v_d(t)}{nV_T}\right) \tag{5.19}$$

- Valid for signals whose amplitudes are sufficiently small, e.g., $10mV$ for the case $n = 2$ and $5mV$ for $n = 1$.[4]
- The ac current in Eq. (5.19), defined as follows, is proportional to the signal $v_d(t)$.

$$i_d(t) \equiv I_D \times \frac{v_d(t)}{nV_T} \tag{5.20}$$

- The diode small-signal resistance (or incremental resistance)[5], $v_d(t)/i_d(t) =$

[3]The fourier expansion of $e^x =$.
[4]The magnitude is approximately $(1/5) \times nV_T$.
[5]Only the ac component is considered.

nV_T/I_D, is inverse proportional to the bias current I_D.

Conclusion 5.3 *For diode, the small signal analysis can be performed separately from the dc analysis.*

- After the dc analysis is performed, the small signal equivalent circuit is obtained by eliminating all dc sources (i.e., short-circuiting dc voltage sources and open-circuiting ac current sources.) and replacing the diode with its small-signal resistance.

Example 5.4 *Consider the circuit shown in Figure 5.16 (a) for the case in which* $R = 10K\,\Omega$. *The power supplier* V^+ *has a dc value of 10V on which it is superimposed a 60Hz sinusoid of 1-V peak amplitude. Calculate the dc voltage of the diode and the amplitude of the sine-wave signal appearing across it. Assume the diode to have a 0.7-V drop at 1-mA current and n=2.*

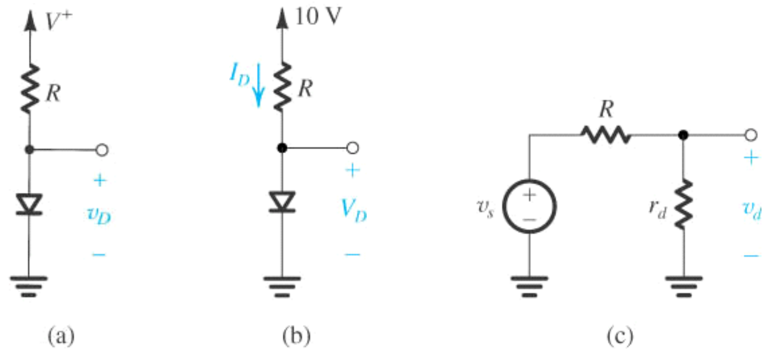


Figure 5.16: Example of separating small signal analysis from dc analysis.

1. Consider dc signal only as in Figure 5.16 (b), the dc current of the diode is

$$I_D = \frac{10 - 0.7}{10} = 0.93mA$$

2. Since the dc current is very close to $1mA$, the diode voltage will be very close to the assumed $0.7V$. At this quiescent point, the diode incremental resistance γ_d is

$$\gamma_d = \frac{nV_T}{I_D} = \frac{2 \times 25}{0.93} = 53.8\,\Omega$$

3. Now we remove the dc source and replace the diode with incremental resistance as in Figure 5.16 (c). Then, the peak amplitude of v_d can be calculated as follows.

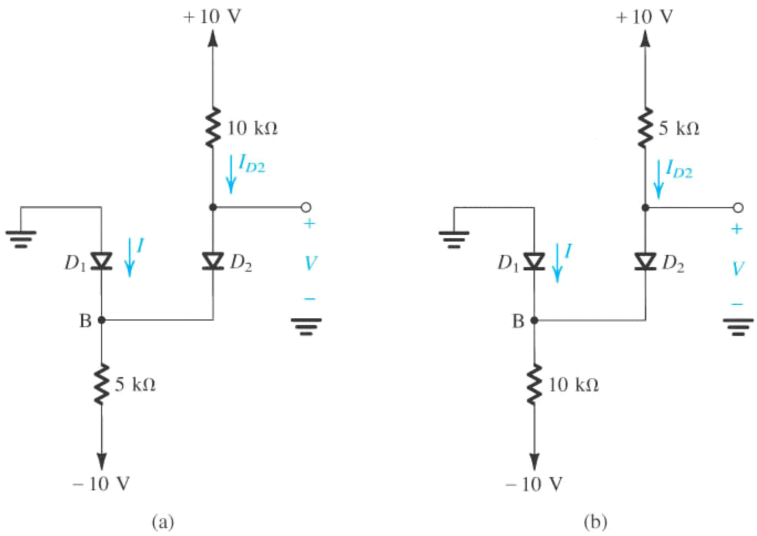
$$v_d(peak) = v_s \times \frac{\gamma_d}{R + \gamma_d} = 5.35mV.$$

4. As compared with $nV_T = 50mV$, the peak amplitude of v_d is quite small. The use of the small-signal model is justified.

5.3.3 Circuit Analysis with Diodes

Analysis of a circuit including diodes normally goes through the following procedure.

- Make plausible assumptions.
- Apply linear circuit analysis.
- Check solution and repeat the process if necessary.



Example 5.5 *Resolve the current I and the voltage V for the two circuits in Figure* **??**.

Case A

1. Diodes D_1 and D_2 are assumed to be forward biased and replaced with short circuits. It follows that $V_B = 0$ and $V = 0$. Consequently,

$$I_{D2} = \frac{10 - 0}{10} = 1\text{mA}.$$

2. Further, writing a node equation at the node B.

$$I + 1 = \frac{0 - (-10)}{5} \Rightarrow I = 1\text{mA}.$$

3. Thus, both D_1 and D_2 are conducting as originally assumed.

Case B

1. Diodes D_1 and D_2 are assumed to be forward biased and replaced with short circuits. It follows that $V_B = 0$ and $V = 0$. Consequently,

$$I_{D2} = \frac{10 - 0}{5} = 2\text{mA}.$$

2. Further, writing a node equation at the node B.

$$I + 2 = \frac{0 - (-10)}{10} \Rightarrow I = -1\text{mA}.$$

3 Since this is not possible, the assumption is invalid. To obtain a consistent solution, the assumption is modified in such a way that D_1 is off. As a result,

$$I_{D2} = \frac{10 - (-10)}{15} = 1.33\text{mA}.$$

$$V = V_B = -10 + 1.33 \times 10 = 3.3\text{V}.$$

5.4 Special Diodes

5.4.1 Zener diode

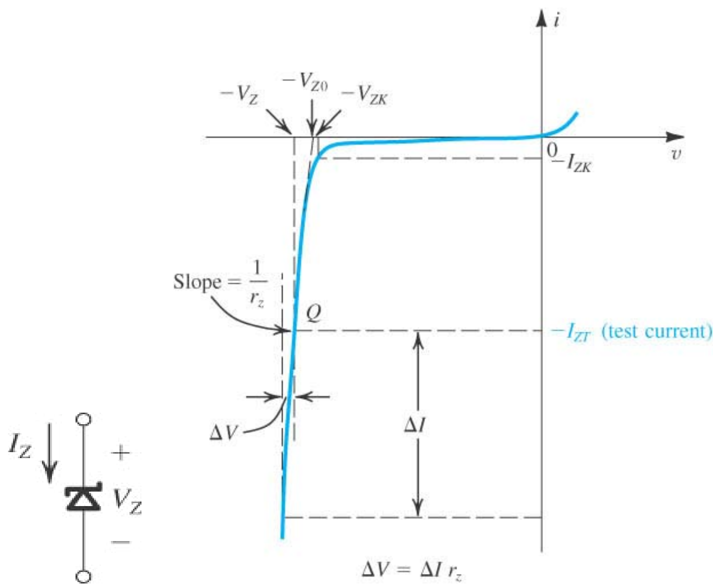


Figure 5.17: Symbol of Zener diode and its i-v characteristics.

- Zener diodes are specifically designed to operate in breakdown region.
  - The steep $i - v$ characteristic is ideal for voltage regulators[6].

[6]Voltage regulators need to provide constant dc output voltages in the face of changes in load current and system power-supply voltage.

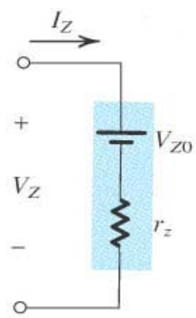


Figure 5.18: Model for the Zener diode.

- Parameters of Zener diodes.
  - The voltage V_Z across the diode at a testing current I_{ZT}. (The operating point)
  - The incremental resistance γ_z at the operation point.
  - The knee current I_{ZK}.
    - The $i - v$ curve for currents greater than I_{ZK} is almost a straight line.
- Model of Zener diodes in breakdown region is specified in Eq. (5.21).
  - Applied for $I_Z > I_{ZK}$ and $V_Z > V_{Z0}$.
  - V_{Z0} is the intersection of the straight line of slope $1/\gamma_z$ and the voltage axis.

$$V_Z = V_{Z0} + \gamma_z I_Z \tag{5.21}$$

5.4.2 Switching Controlled Rectifier (SCR)

5.4.3 LED/Varactors

5.5 Applications

5.5.1 Regulator

Example 5.6 *Use of the Zener diode as a Shunt Regulator which appears in parallel with the load. The 6.8-V Zener diode in Figure 5.19 is specified to have* $V_Z = 6.8V$ *at* $I_Z = 5mA$,$\gamma_Z = 20\,\Omega$, *and* $I_{ZK} = 0.2mA$.*The supply voltage* V^+ *is normally* $10V$ *but can vary by* $\pm 1V$.

1. From Eq. (5.21) and the given conditions, V_{Z0} can be derived as $6.7V$.
2. The V_o with no loading.

$$\begin{aligned} I_Z &= I = \frac{10 - 6.7}{0.5 + 0.2} = 6.35mA \\ V_o &= V_{Z0} + \gamma_Z \times I_Z = 6.83V \end{aligned}$$

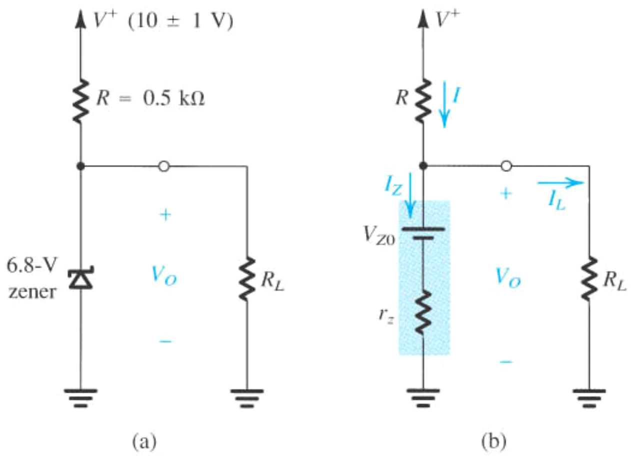


Figure 5.19: Use of Zener diode as a Shut Regulator.

3. The line regulation ($\Delta V_o/\Delta V^+$) due to the $\pm 1V$ change of power supply.

$$\begin{aligned}\Delta V_o &= \Delta V^+ \times \frac{\gamma_Z}{R+\gamma_Z}\\ \frac{\Delta V_o}{\Delta V^+} &= \frac{\gamma_Z}{R+\gamma_Z} = \frac{20}{500+20} = 38.5mV/V\end{aligned}$$

4. The load regulation ($\Delta V_o/\Delta I_L$) as a load resistor draws a current $I_L = 1mA$.
   - Assume the total current I does not change significantly when the load is connected.

$$\begin{aligned}\Delta V_o &= \gamma_Z \times \Delta I_Z = 20 \times -1 = -20mV.\\ \frac{\Delta V_o}{\Delta I_Z} &= -20mV/mA\end{aligned}$$

5. The change of V_o when a load resistor $R_L = 2K\,\Omega$ is connected.
   - Assume the total current I does not change significantly when the load is connected.
   - The approximation of the load current is as follows and the change of V_o can be obtained accordingly.

$$\begin{aligned}\Delta I_Z &= \frac{6.8}{2} = 3.4mA.\\ \Delta V_o &= \gamma_Z \times \Delta I_Z = 20 \times -3.4 = -68mV.\end{aligned}$$

   - The accurate number from circuit analysis is $\Delta V_o = -70mV$.
6. The change of V_o when a load resistor $R_L = 0.5K\,\Omega$ is connected.
   - It is impossible that the load would draw a current of $6.8/0.5 = 13.6mA$. Thus,

the diode must be cut-off. Accordingly, the V_o can be obtained as follows:

$$V_o = V^+ \times \frac{R}{R + R_L} = 5V.$$

7. The minimum value of R_L for which the diode still operates in the breakdown region.
   - The minimum voltage supply is around $9V$. At this point, the lowest current supplied is $(9 - 6.7)/0.5 = 4.6mA$ and thus the load current is $4.6 - 0.2 = 4.4mA$. The corresponding value of $R_L = 6.7/4.4 = 1.5K\,\Omega$.

5.5.2 Rectifier

- A diode rectifier is an essential building block of the dc power supply.
- Figure 5.20 depicts the block diagram of the dc power supply.
  - Power transformer
    - To step the line voltage down to the required value.
    - To minimize the risk of electric shock by providing electrical isolation between the equipment and the power line.
  - Diode rectifier
    - Convert input sinusoid to a unipolar output.
    - Two parameters must be specified in selecting the diodes.
      - The largest current the diode is expected to conduct.
      - The largest reverse current that is expected to withstand without breakdown. (Peak inverse voltage)
  - Filter
    - Convert pulsating waveform to a constant output.
  - Voltage regulator
    - To reduce the ripple
    - To stabilize the dc output as the load current changes.

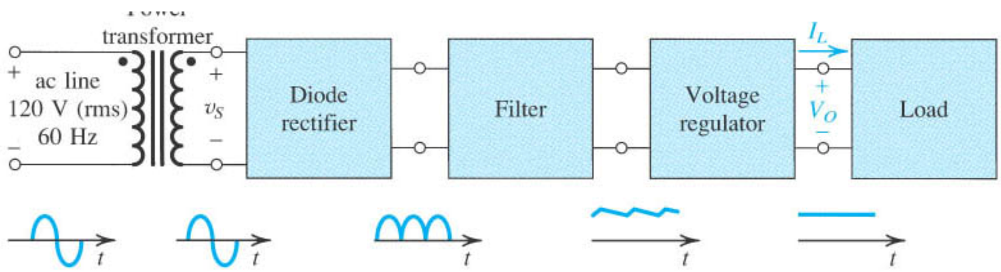


Figure 5.20: Block diagram of a dc power supply.

Half-Wave Rectifier

- Utilize alternate half-cycles of the input sinusoid.
- Figure 5.21 shows an example of half-wave rectifier.
  - PIV= V_S.
  - It may not function properly when the input signal is small.

$$v_o = \begin{cases} 0 & if \quad V_S < V_{D0} \\ \frac{R}{R+\gamma_D} \times (V_S - V_{D0}) & if \quad V_S \geq V_{D0} \end{cases} . \tag{5.22}$$

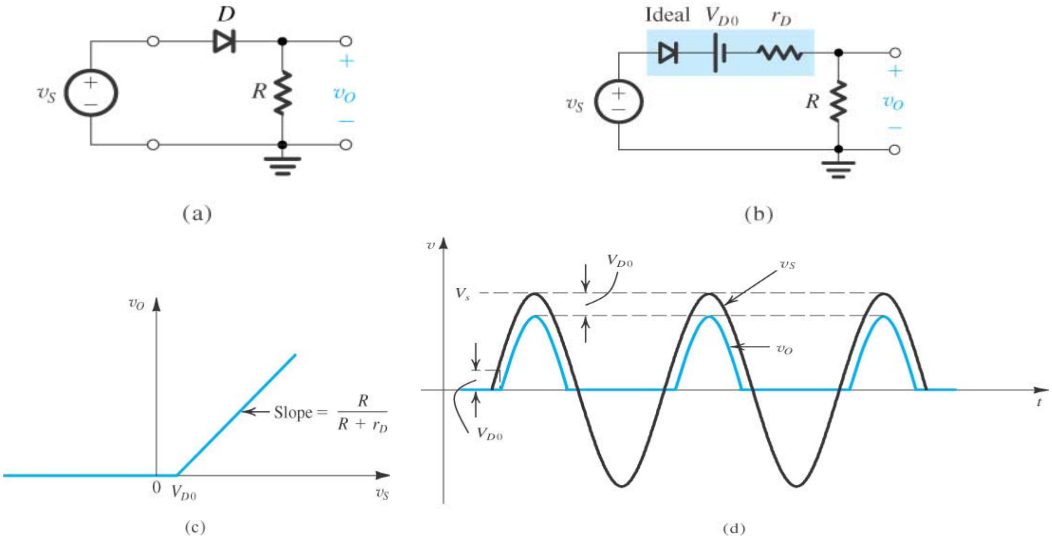


Figure 5.21: Circuit of half-wave rectifier.

Full-Wave Rectifier

- Utilize both halves of the input sinusoid.
- Figure 5.22 shows an example of full-wave rectifier.
  - When the input voltage is positive, both of the signals v_S will be positive.
    - D_1 will conduct and D_2 will be reverse biased.
  - When the input voltage is negative, both of the signals v_S will be negative.
    - D_1 will be reverse biased and D_2 will conduct.
  - v_o is unipolar since the current always flows through R in the same direction.
  - PIV= $2V_S - V_D$.
  - A center-tapped transform is required.
- Figure 5.23 shows another implementation of full-wave rectifier.
  - When the input voltage is positive, the signals v_S will be positive.
    - D_1 and D_2 will conduct; D_3 and D_4 will be reverse biased.
  - When the input voltage is negative, the signals v_S will be negative.

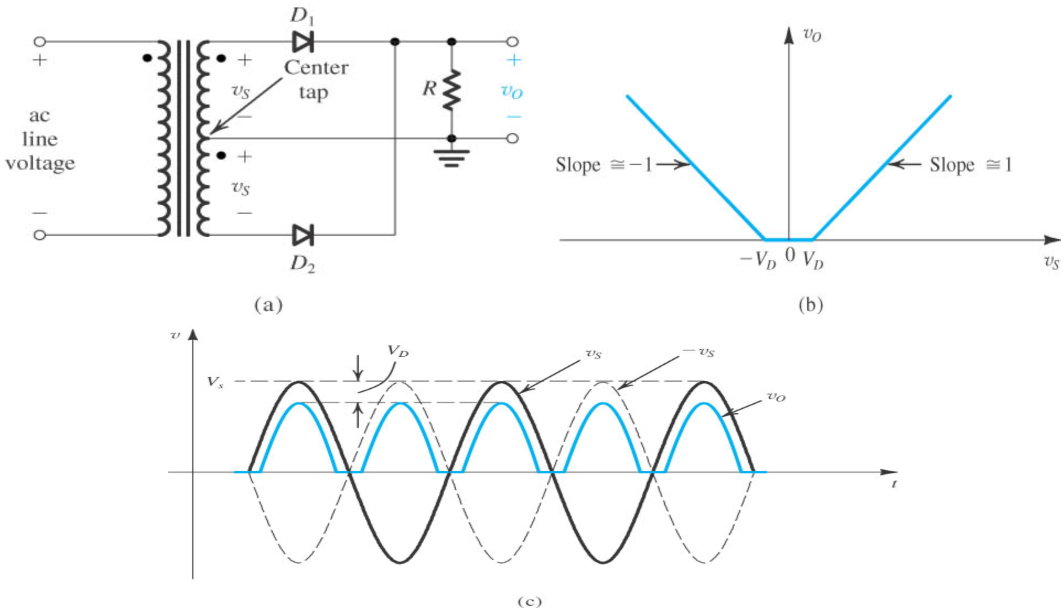


Figure 5.22: Circuit of full-wave rectifier using center-tapped transformer.

    * D_3 and D_4 will conduct; D_1 and D_2 will be reverse biased.
  - v_o is unipolar since the current always flows through R in the same direction.
  - PIV= $v_o + v_{D2}$(forward)= $V_S - 2V_D + V_D = V_S - V_D$.
  - Advantages
    * PIV is about half the value for the center-tapped implementation.
    * A center-tapped transform is not required.
    * Less turns are required for the secondary winding of the transformer.

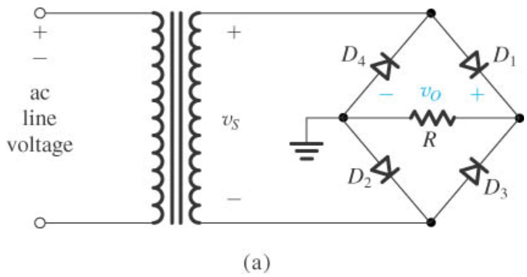


Figure 5.23: Circuit of the bridge rectifier.

The Peak Rectifier

- The peak rectifier reduces the variation of output voltage by introducing a capacitor.
- Figure 5.24 shows the circuit of the peak rectifier.
  - The capacitor charges to the peak of the input V_P.
  - The diode cuts off and the capacitor discharges through the load R.

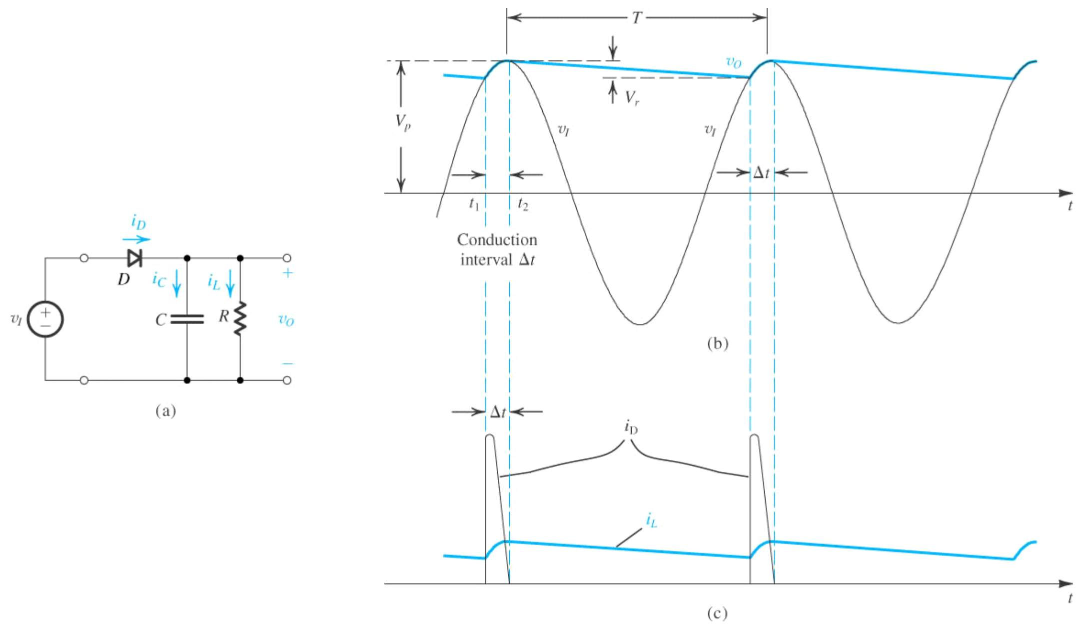


Figure 5.24: Circuit of the peak rectifier.

∗ The output $v_o(t)$ during the discharge.[7]

$$v_o(t) = V_P e^{-t/RC} \tag{5.23}$$

∗ The voltage drop V_γ due to the discharge.[8]

$$\begin{aligned} V_P - V_\gamma &\simeq V_P e^{-T/RC} \\ \Rightarrow \quad V_\gamma &= V_P(1 - e^{-T/RC}) \simeq V_P \frac{T}{RC} \end{aligned} \tag{5.24}$$

· To keep V_γ small, we must select a capacitor C so that $RC \gg T$.

∗ The alternative expression of V_γ.

$$V_\gamma \simeq V_P \frac{T}{RC} = \frac{I_L}{fC} \tag{5.25}$$

· $I_L = V_P/R$ is the load current when V_γ is small.

· $f = 1/T$ is the frequency of the voltage supplier.

· To keep V_γ small, we can either select a large capacitor C or increase the frequency of the voltage supplier.

– The discharge continues until v_I exceeds the capacitor voltage.

[7] The node equation when the diode is cut off: $C\frac{dv_o(t)}{dt} + \frac{v_o(t)}{R} = 0$.
[8] $e^x =$

5.5.3 Limiting

- Limiter (also known as clipper) limits the voltage between the two output terminals.

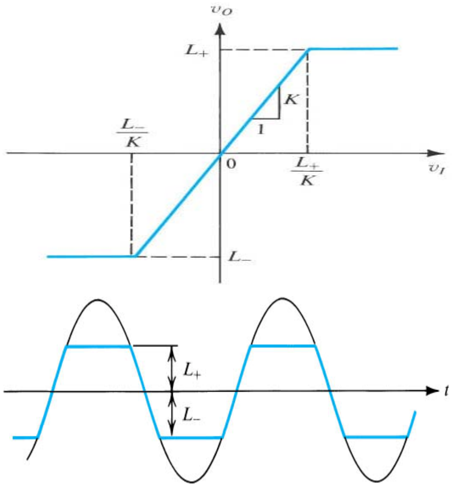


Figure 5.25: Transfer characteristic for a limiter circuit.

- Eq. (5.26) and Figure 5.25 show the transfer function of limiter.

$$v_o = \begin{cases} L_- & if \quad v_I < L_-/K \\ Kv_I & if \quad L_-/K \leq v_I \leq L_+/K \\ L_+ & if \quad v_I > L_+/K \end{cases} . \tag{5.26}$$

- Diode can be combined with resistors to implement limiters.
  - Figure 5.26 (a) and (b) are single limiters.
    - Single limiter works for either positive or negative peak.
  - Figure 5.26 (c) is a double limiter.
    - Double limiter works for both positive and negative peaks.
  - Figure 5.26 (d) shows that the threshold and saturation current can be controlled by using strings of diodes and/or by connecting a dc voltage in series with the diode.
  - Figure 5.26 (e) shows another double limiter using double-anode Zener.

5.5.4 Clamping

- Diodes can be used for the circuit of dc restorer (also known as clamped capacitor).
- Figure 5.27 shows an example of dc restorer with no load.
  - When $v_I = -6V$, the capacitor will charge to a voltage v_C.
    - v_C is equal to the magnitude of the most negative peak, i.e., $6V$.
    - The polarity of v_C is indicated as in Figure 5.27.

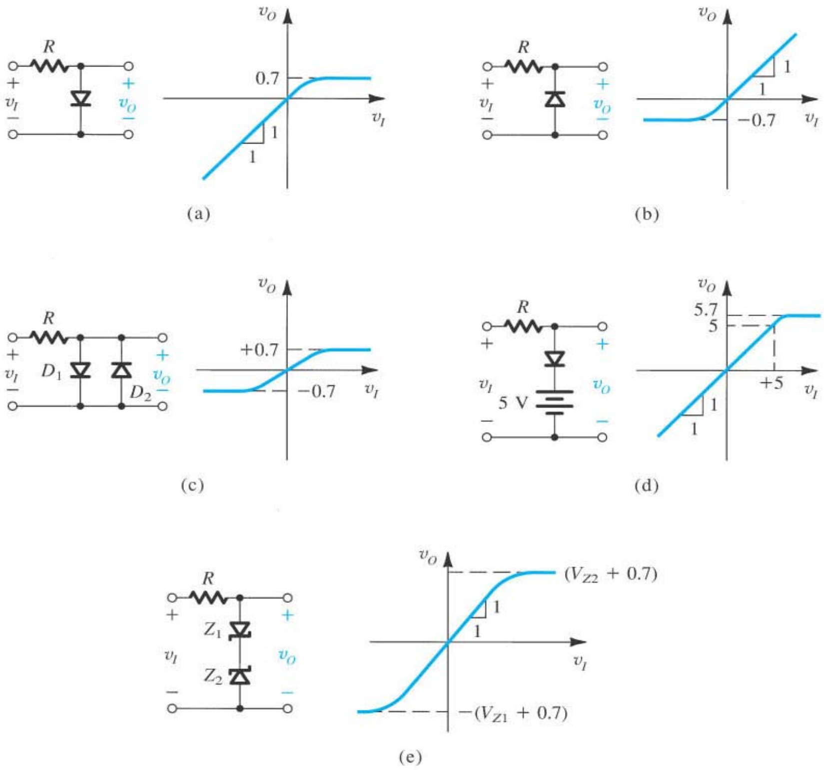


Figure 5.26: A varity of basic limiting circuits.

  - ∗ The diode is turned off and the capacitor retains its voltage indefinitely.
- – When $v_I = 4V$, the output $v_C = v_I + v_C = 10V$.
- Figure 5.28 shows the example of dc restorer with a load resistor R.
  - – As $t_0 < t < t_1$, the output voltage falls exponentially with time constant RC.
  - – At t_1, the input decreases by V_a and the output attempts to follow.
    - ∗ The diode conduct heavily and quickly discharge the capacitor.
  - – At the end of the period t_1 to t_2, the output voltage is around $-0.5V$.

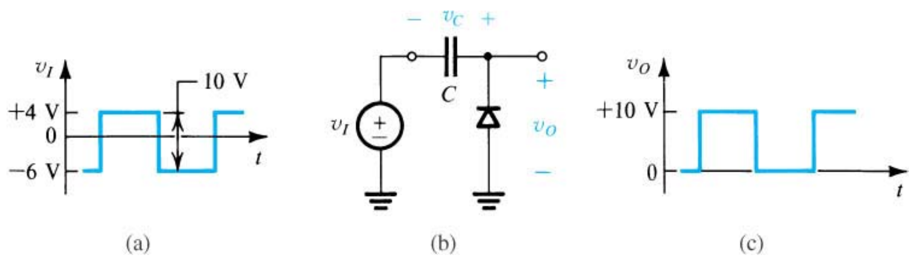


Figure 5.27: The clamped capacitor or dc restorer with a square-wave input and no load.

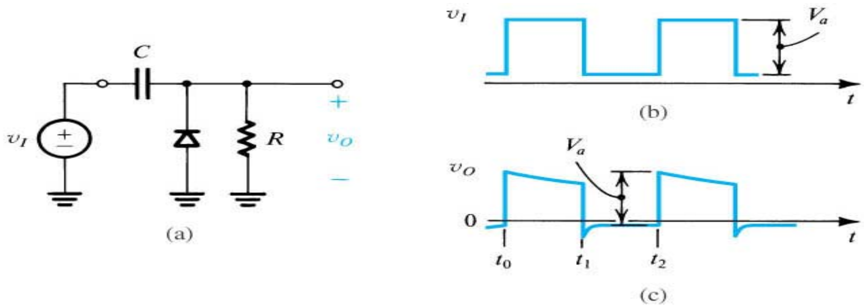


Figure 5.28: The dc restorer with a load resistor R.

5.5.5 Digital Logic

- Diodes can also be used for logic gates as shown in Figure 5.29.

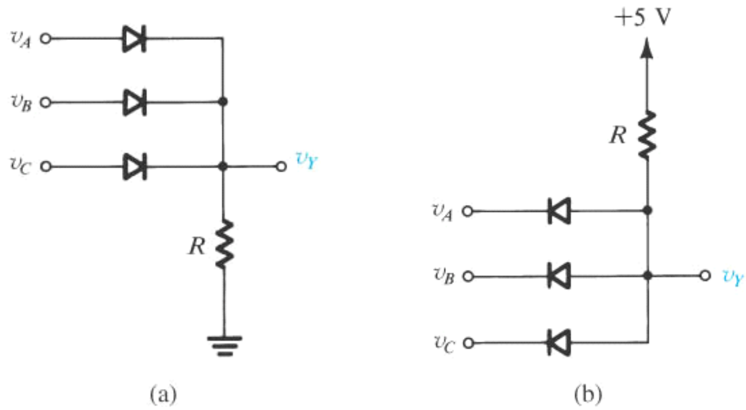


Figure 5.29: Digital logic gates: (a) OR gate; (b) AND gate. (Positive logic system)